PATENT APPLICATION - CERTIFICATE OF MAILING

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Title of Invention: **NON-VOLATILE MEMORY CELL COMPRISING DIELECTRICLAYERS HAVING A LOW DIELECTRIC CONSTANT AND CORRESPONDING MANUFACTURING PROCESS**

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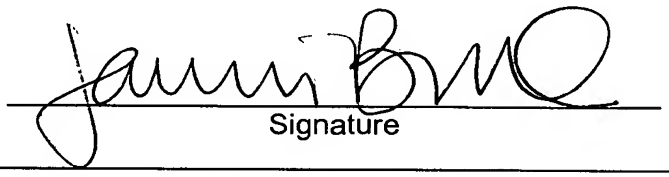

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Enclosures:

- Utility Application Transmittal
- Specification and Claims (15 pages)
- Drawings (3 pages)
- Return postcard

NON-VOLATILE MEMORY CELL COMPRISING DIELECTRICLAYERS HAVING A LOW DIELECTRIC CONSTANT AND CORRESPONDING MANUFACTURING PROCESS

PRIORITY CLAIM

[1] This application claims priority from European patent application No. 02425805.5, filed December 30, 2002, which is incorporated herein by reference.

TECHNICAL FIELD

[2] The present invention relates to a non-volatile memory cell comprising dielectric layers having low dielectric constant and corresponding process.

[3] More specifically, an aspect of the invention relates to a non-volatile memory cell integrated on a semiconductor substrate and comprising:

a floating gate transistor including a source region and a drain region, a gate region projecting from the substrate and comprised between said source and drain regions, said gate region having a predetermined length and width and comprising a first floating gate region and a control gate region.

[4] Another aspect of the invention relates also to a process for manufacturing non-volatile memory cells on a semiconductor substrate, comprising the following steps:

form active areas in said semiconductor substrate bounded by an insulating layer,

form on said active areas a first dielectric material layer,

deposit a first conductor material layer on said first dielectric layer,

define through a standard photolithographic technique a plurality of floating gate regions.

[5] The described embodiments of the invention relate particularly, but not exclusively, to a Flash non-volatile memory cell comprising dielectric layers with low dielectric constant and the following description is made with reference to this field of application for convenience of illustration only.

BACKGROUND

[6] As it is well known, semiconductor-integrated Flash EPROM memory electronic devices comprise a plurality of matrix-organized non-volatile memory cells ***1***; i.e. that cells are organized according to rows, referred to as word lines ***WL***, and columns, referred to as bit lines ***BL***, as shown in **FIG. 1a**.

[7] Each non-volatile cell ***1*** comprises a floating gate ***MOS*** transistor as shown in **FIG. 1b**. The floating gate region ***FG*** of the floating gate transistor is formed above the channel region ***CH*** formed in the semiconductor substrate ***2*** and separated from the latter through a thin oxide layer ***3*** (tunnel oxide) being about ~10 nm thick. A control gate region ***CG*** is coupled in a capacitive way to the floating gate region ***FG*** through a single dielectric layer ***7*** or comprising several overlapped dielectric layers such as for example ONO (oxide/nitride/oxide).

[8] The other transistor regions are the usual drain, source and body terminals. Metallic electrodes are provided to contact the drain and source terminals and the control gate region ***CG*** in order to allow predetermined voltage values to be applied to the memory cell ***1***.

[9] The charge stored in the floating gate region ***FG*** determines the logic state of cell ***1*** by modifying the threshold voltage thereof: in fact a fundamental feature of the memory cell ***1*** is to have two states, the one with a low threshold voltage ("erased" cell) and the other with a high threshold voltage ("written" cell). The voltage is applied from the outside to the control gate region ***CG***, but the electrode which effectively controls the channel state is the floating gate region ***FG***.

[10] A known process flow to manufacture Flash memory cells ***1*** integrated on a semiconductor substrate ***2*** is shown in **FIGS. 2 to 5**. These figures are vertical section views in a parallel direction to "Word Lines".

[11] This known process provides that in the substrate a plurality of active areas, wherein memory cells will be formed, separated from each other by portions of a field oxide layer ***FOX***, are formed. A first dielectric layer ***3*** referred to as "Tunnel Oxide" and a polycrystalline silicon layer ***4*** referred to as POLY1 are then formed on the substrate ***2***.

[12] This polycrystalline silicon layer ***4*** which is about 50-200 nm thick is formed

for example through LPCVD (Low Pressure Chemical Vapor Deposition). This polycrystalline silicon layer ***4*** is, in case, doped to reduce the resistivity thereof, for example through a phosphorus or arsenic implant or in situ by adding phosphin to the deposition environment.

[13] The process continues with the definition of layer ***4*** to form a plurality of polycrystalline silicon strips ***5*** being parallel to each other. These strips ***5*** are separated and insulated from the substrate ***2*** by means of the oxide layer ***3*** as shown in **FIG. 3**.

[14] Particularly, in this step, a photosensitive material layer ***6*** referred to as resist is deposited on the substrate ***2*** surface and it is exposed to a convenient radiation in predetermined areas which are not protected by a mask. The resist portions selectively exposed to the radiation have a higher removing speed than the non-exposed regions and they can thus be removed through a chemical solution referred to as developer. After the lithographic definition a dry etching of the polycrystalline silicon strips ***5*** is performed to define the floating gate regions ***FG***.

[15] After depositing an interpoly dielectric layer ***7***, the standard process flow continues with the "Word Line" definition by forming a polycrystalline silicon layer ***8*** (referred to as Poly2).

[16] "Word Lines" are thus defined through a photolithographic process providing the use of a resist mask so that these word lines are located perpendicularly to the polysilicon strips ***5***.

[17] Although advantageous under many aspects, this process flow has several drawbacks. In fact the area between two adjacent floating gates is completed with the deposition of the second polysilicon layer ***8***. Cell ***1*** is then filled up by dry etching.

[18] Nevertheless, the decrease in size of the area between two adjacent floating gates (~ 40-50 nm in the most advanced technologies) makes the filling with a material like polysilicon difficult.

[19] It must be added that the interpoly dielectric layer ***7*** like ONO, being a high dielectric constant K material, increases the capacitive coupling between adjacent

floating gate regions ***FG***. This can cause undesired interactions between adjacent cells, especially if they are in different logic states.

[20] The technical problem underlying embodiments of the present invention is to provide a method for forming non-volatile memory cells, having such structural and functional characteristics as to allow the capacitive coupling between adjacent floating gate regions to be reduced, overcoming thus the limits that currently affect devices manufactured according to the prior art.

SUMMARY

[21] A solutive idea underlying an aspect of the present invention is to define a process sequence needed to obtain a memory device organized in rows and columns comprising non-volatile memory cells wherein the area between two adjacent floating gate regions belonging to the same row is filled up with low dielectric constant (low-k) material.

[22] On the basis of this solutive idea, according to one aspect of the present invention the technical problem is solved by a memory cell as previously described and defined in the characterising part of claim 1.

[23] According to another aspect of the present invention, the problem is solved also by a process as previously described and defined in the characterising part of claim 7.

[24] The features and advantages of devices according to various aspects of the invention will be apparent from the following description of an embodiment thereof given by way of non-limiting example with reference to the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[25] **FIG. 1a** is a schematic view of a memory cell matrix portion in a semiconductor-integrated memory electronic device;

[26] **FIG. 1b** is a sectional view along the line I-I of **FIG. 1** of a standard memory cell;

[27] **FIG. 1c** is a sectional view along the line II-II of **FIG. 1** of a standard memory

cell;

[28] **FIGS. 2 to 5** show respective vertical sections in an enlarged scale of a semiconductor substrate portion during a process for manufacturing non-volatile memory cells according to the prior art;

[29] **FIGS. 6 and 7** show respective vertical sections in an enlarged scale of a semiconductor substrate portion during a process for manufacturing non-volatile memory cells according a first embodiment of the invention;

[30] **FIGS. 8 and 9** show respective vertical sections in an enlarged scale of a semiconductor substrate portion during a process for manufacturing non-volatile memory cells according to a second embodiment of the invention.

DETAILED DESCRIPTION

[31] The following discussion is presented to enable a person skilled in the art to make and use the invention. Various modifications to the embodiments will be readily apparent to those skilled in the art, and the generic principles herein may be applied to other embodiments and applications without departing from the spirit and scope of the present invention. Thus, the present invention is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features disclosed herein.

[32] With reference to **FIGS. 6 to 9**, a floating gate memory cell ***1*** insulated through dielectric layers with low dielectric constant K value is described.

[33] A corresponding manufacturing process of this cell ***1*** is also described.

[34] The process steps described hereafter do not form a complete process flow for manufacturing integrated circuits. The described embodiments of the present invention can be implemented together with the techniques for manufacturing integrated circuits currently used in this field, and only those currently used process steps which are necessary for understanding these embodiments of the present invention are included.

[35] The figures which are schematic views of portions of an integrated circuit during the manufacturing thereof are not drawn to scale, but they are instead drawn so as to show the important features of the described embodiments of the present

invention.

[36] As described for the prior art, each non-volatile cell ***1*** comprises a floating gate MOS transistor. The floating gate region ***FG*** of the floating gate transistor is formed above the channel region ***CH*** formed in the semiconductor substrate ***2*** and separated by the latter through a thin oxide layer ***3*** (tunnel oxide), being 6-12 nm thick. A control gate region ***CG*** is coupled in a capacitive way to the floating gate region ***FG*** through a single dielectric layer ***5*** or comprising several overlapped dielectric layers such as for example ONO (oxide-nitride-oxide).

[37] According to an embodiment of the invention, a dielectric layer ***9*** with low dielectric constant is formed between floating gate regions ***FG*** belonging to the same memory cell matrix row in order to reduce the coupling between adjacent cells ***1***.

[38] After all, this dielectric layer ***9*** with low dielectric constant insulates a floating gate region ***FG*** from the adjacent regions along the direction of the memory cell width W.

[39] A process for forming a memory cell ***1*** according to an embodiment of the invention is now described.

[40] On a substrate ***2*** a plurality of active areas are formed, wherein memory cells ***1***, separated from each other by portions of a field oxide layer ***FOX***, will be formed. A first active dielectric layer ***3*** and a layer ***4*** made of a conductor material, like for example polycrystalline silicon referred to as POLY1, are then formed on the substrate ***2***.

[41] Advantageously, this first active dielectric layer ***3*** is an oxide layer referred to as "Tunnel Oxide" and it is formed on the substrate ***2*** through a thermal oxidation step.

[42] This polycrystalline silicon layer ***4*** being about 50-200 nm thick is formed for example through LPCVD (Low Pressure Chemical Vapor Deposition). This polycrystalline silicon layer ***4*** is, in case, doped to reduce the resistivity thereof, for example through a phosphorus or arsenic implant or in situ by adding phosphin to the deposition environment.

[43] The process continues with the definition of layer ***4*** to form a plurality of polycrystalline silicon strips ***5*** being parallel to each other. These strips ***5*** are separated and insulated from the substrate ***2*** by means of the oxide layer ***3*** as shown in **FIG. 3**.

[44] Particularly, in this step, a photosensitive material layer ***6*** referred to as resist is deposited on the substrate ***2*** surface and it is exposed to a convenient radiation in predetermined areas which are not protected by a mask. The resist portions selectively exposed to the radiation have a higher removing speed than the non-exposed regions and they can thus be removed through a chemical solution referred to as developer. After the lithographic definition a dry etching of the polycrystalline silicon strips ***5*** is performed to define the floating gate regions ***FG***.

[45] Advantageously, a first oxidation step, for example a RTO (Rapid Thermal Oxidation), is performed in a dry environment, obtaining a first very thin dielectric layer of about 1-2 nm, not shown in figures. This first dielectric layer is capable of protecting the walls of the floating gate region ***FG***.

[46] A layer ***9*** made of a low dielectric constant K material is then formed in order to fill up an area between two adjacent floating gate regions ***FG*** belonging to a same small-sized row.

[47] This layer ***9*** made of a low dielectric constant material is a layer made of an organic or inorganic material such as for example a silicon oxide layer being doped for example with fluorine (FSG Fluorinate Silicate Glass having a dielectric constant comprised between 3.3 and 3.7) or with carbon (for example with alkylic groups, k=2.7-3.1).

[48] These dielectric layers ***9*** are advantageously deposited through different techniques such as CVD (Chemical Vapor Deposition), HDPCVD (High-Density Plasma Enhanced Chemical Vapor Deposition) or the so-called spin-on-glass technique.

[49] Particularly, the dielectric layers ***9*** deposited through these latter techniques have also a high planarizing capacity.

[50] Advantageously other dielectric layers ***9*** are used, such as for example

porous silice, with a dielectric constant K which is slightly higher than ***1***.

[51] Advantageously the dielectric layer ***9*** is subjected to a densification process in order to improve the constant dielectric thereof.

[52] A selective back etching step towards the polysilicon layer ***4*** is then performed through CMP or standard back etching techniques in order to leave the floating gate region ***FG*** exposed.

[53] The deposition of an interpoly dielectric layer ***7*** and of a second polysilicon layer ***8***, being for example about 100-400 nm thick, is performed to form the control gate region of cell ***1*** as shown in **FIG. 7**.

[54] A second method for performing the insulation between floating gate regions ***FG*** according to another embodiment of the present invention is shown in **FIGS. 8-9**.

[55] After forming conventionally the floating gate regions ***FG*** as shown in **FIG. 4**, an interpoly dielectric layer ***7*** is formed.

[56] This interpoly dielectric layer ***7*** is a single oxide layer (of silicon or hafnium or tellurium or other equivalent materials) or it comprises several overlapped layers such as for example an ONO layer (oxide-nitride-oxide) being about 10-25 nm thick.

[57] A layer ***9*** made of a low dielectric constant K material is then formed in order to fill up an area between two small-sized adjacent floating gate regions ***FG***.

[58] This layer ***9*** made of a low dielectric constant material is a layer made of an organic or inorganic material as in the previous embodiment.

[59] A selective back etching towards the interpoly dielectric layer and the deposition of the second polysilicon layer being about 150-250 nm thick (**FIG. 9**) are then performed, which can be preceded by a slight oxidation (or deposition of an equivalent layer) which, through a short thermal treatment and a secondary impact on the final thickness of the interpoly dielectric layer, succeeds in insulating the low-k material from the above polysilicon layer, inhibiting the mutual interaction.

[60] This second method is obviously applied when the distance between two adjacent floating gates is higher than twice the effective thickness of the high-k

dielectric layer ***7*** (ONO or other above-mentioned multi-layer materials) deposited on the walls of the floating gate region ***FG***.

[61] In conclusion, the insertion of a layer with low dielectric constant value reduces interaction problems between adjacent floating gate regions ***FG*** caused by the reduction of the area between two adjacent regions ***FG***.

[62] This process is thus particularly advantageous when using dielectric material layers with high dielectric constant value K as interpoly dielectric layers to improve the capacitive couplings in memory cells ***1***.

[63] Flash memory cells formed according to the described embodiments of the present invention may be contained in a FLASH memory device or other integrated circuit including such a FLASH memory device. Moreover, such a FLASH memory device or other integrated circuit may be contained in a variety of different types of electronic systems, such as a computer system.

[64] From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention.